

#13/Drawing
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Kazuo MATSUZAKI, *et al.*

Group Art Unit: 2811

Serial No.: 09/756,686

Examiner: S. Loke

Filed: January 9, 2001

Attorney Docket No.: FUJI:179

For: SEMICONDUCTOR DEVICE EXHIBITING A HIGH BREAKDOWN VOLTAGE AND THE METHOD
OF MANUFACTURING THE SAMEAssistant Commissioner for Patents
Washington, D.C. 20231Certificate of Filing By Facsimile

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number: 703-872-9318

Date: 12/10/02By: M. A. Rossi

Marc A. Rossi

PROPOSED DRAWING AMENDMENT

Sir:

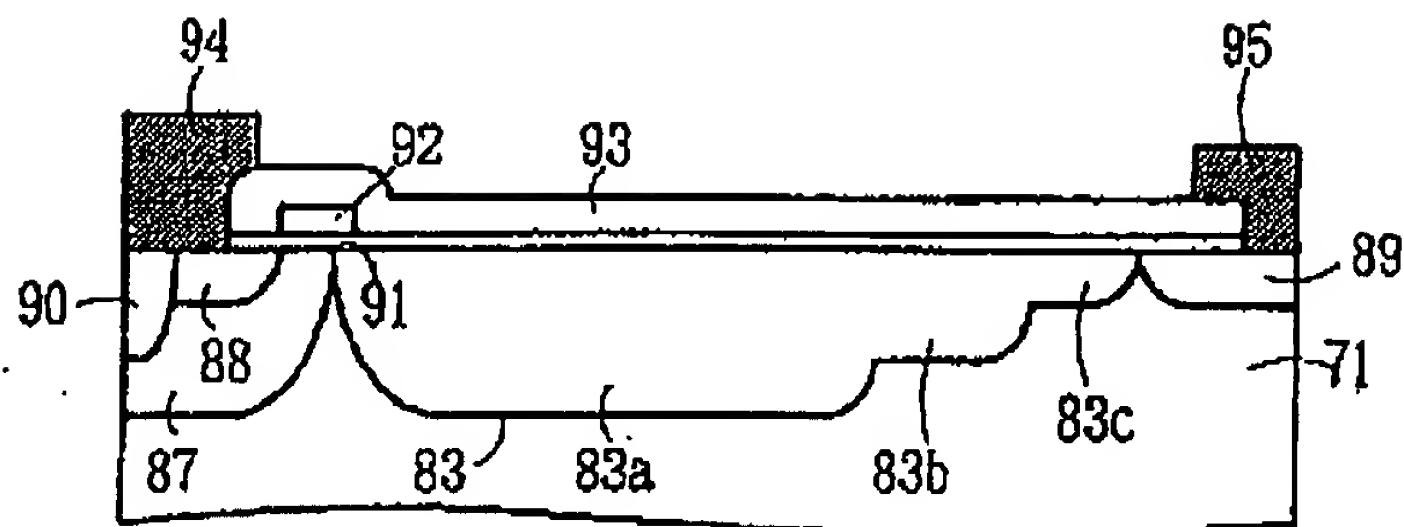
Enclosed for the examiner's approval are copies of Figs. 1 and 3-24(b) with handwritten markings showing the proposed changes, namely removing all extraneous reference descriptions from these figures and including the legend "Prior Art" in Figs. 21, 22(a), 22(b), 23, and 24.

Respectfully submitted,

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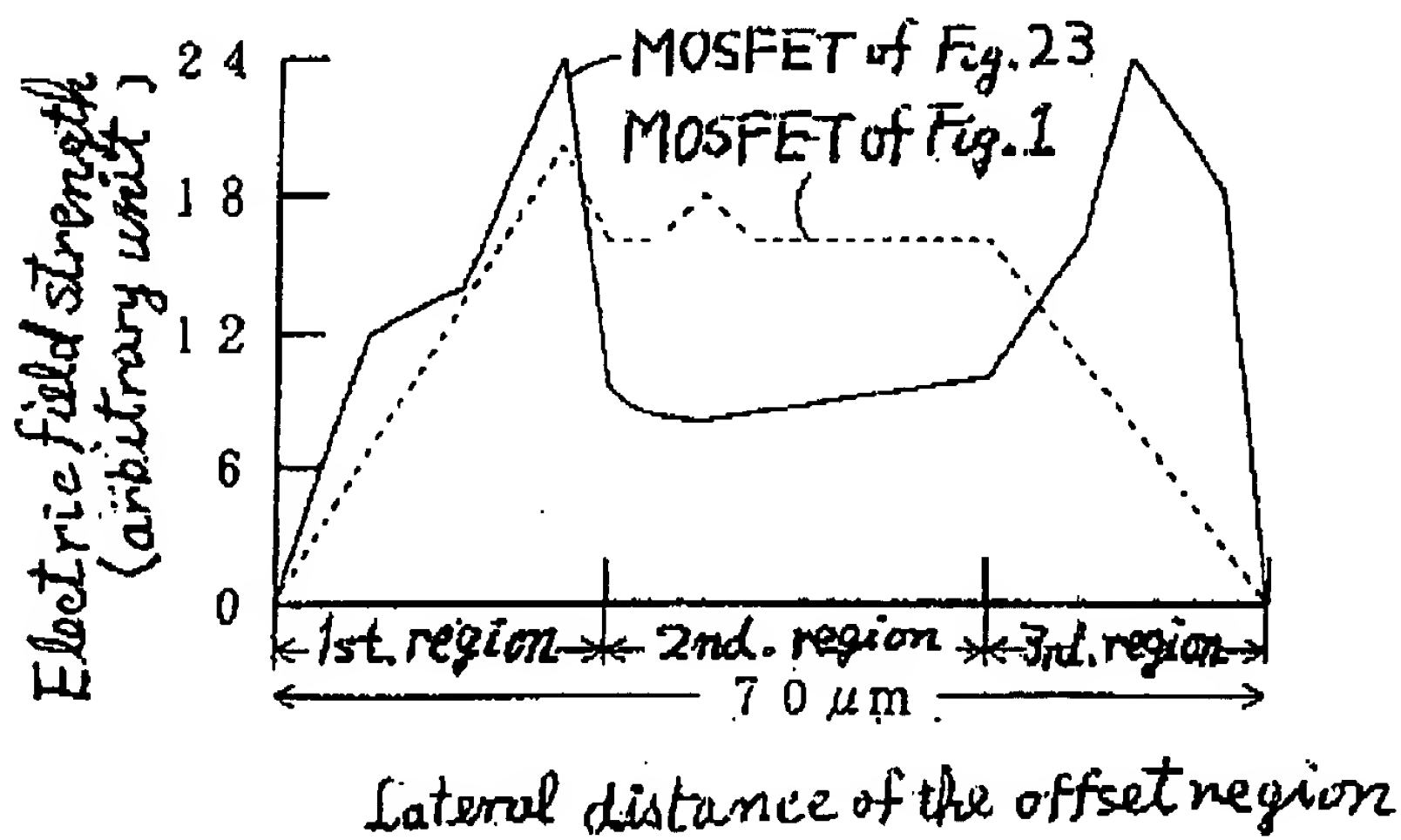
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Fig. 1



- | | |
|-------------------------------|---------------------------|
| 71: n-type silicon substrate | 89: n-type drain region |
| 83: p-type offset region | 90: p-type contact region |
| 83a: First p-type sub-region | 91: Gate insulation film |
| 83b: Second p-type sub-region | 92: Gate electrode |
| 83c: Third p-type sub-region | 93: Insulation film |
| 87: p-type base region | 94: Source electrode |
| 88: n-type source region | 95: Drain electrode |

Fig. 2



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Fig. 3

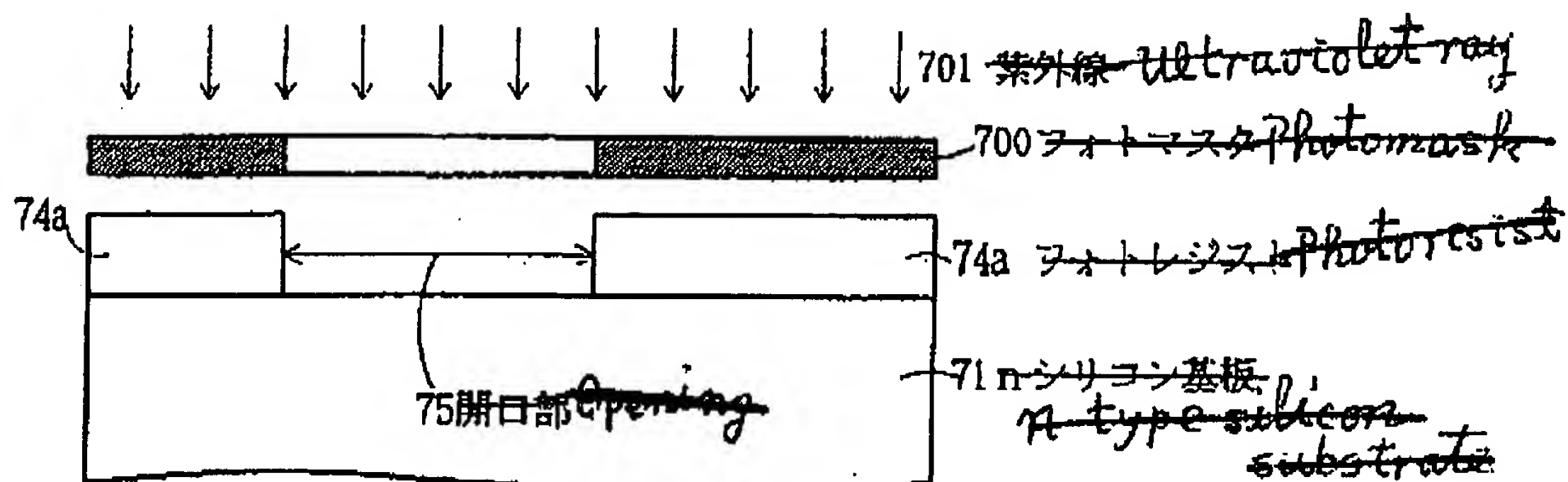


Fig. 4

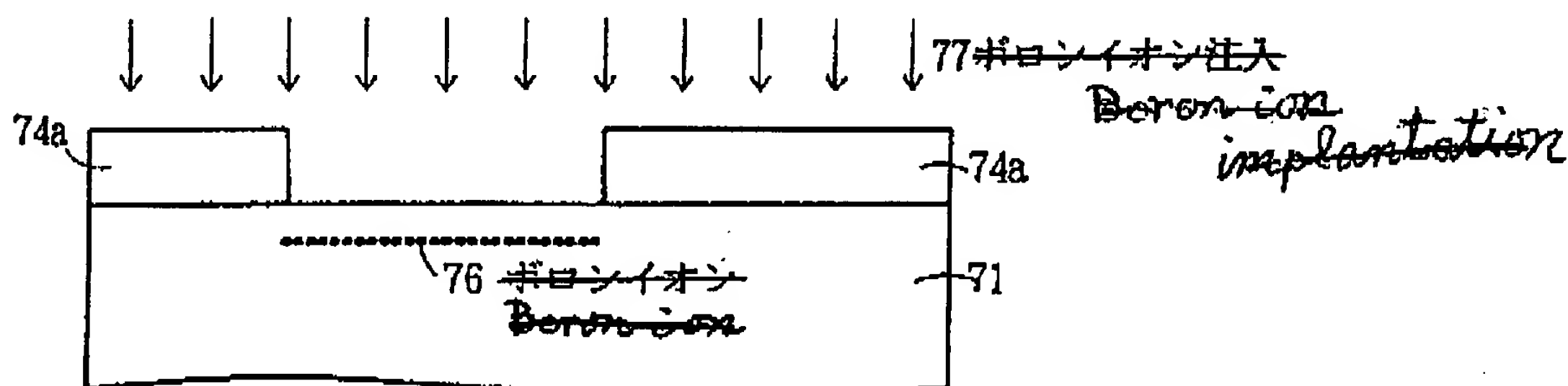
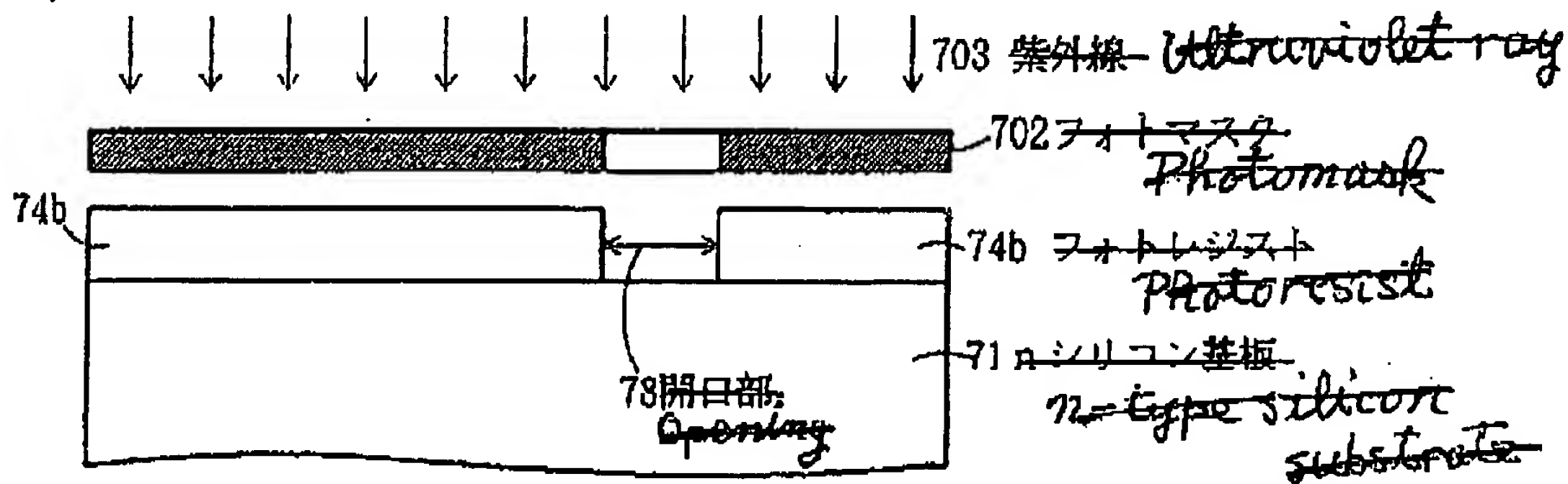


Fig. 5



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Fig. 6

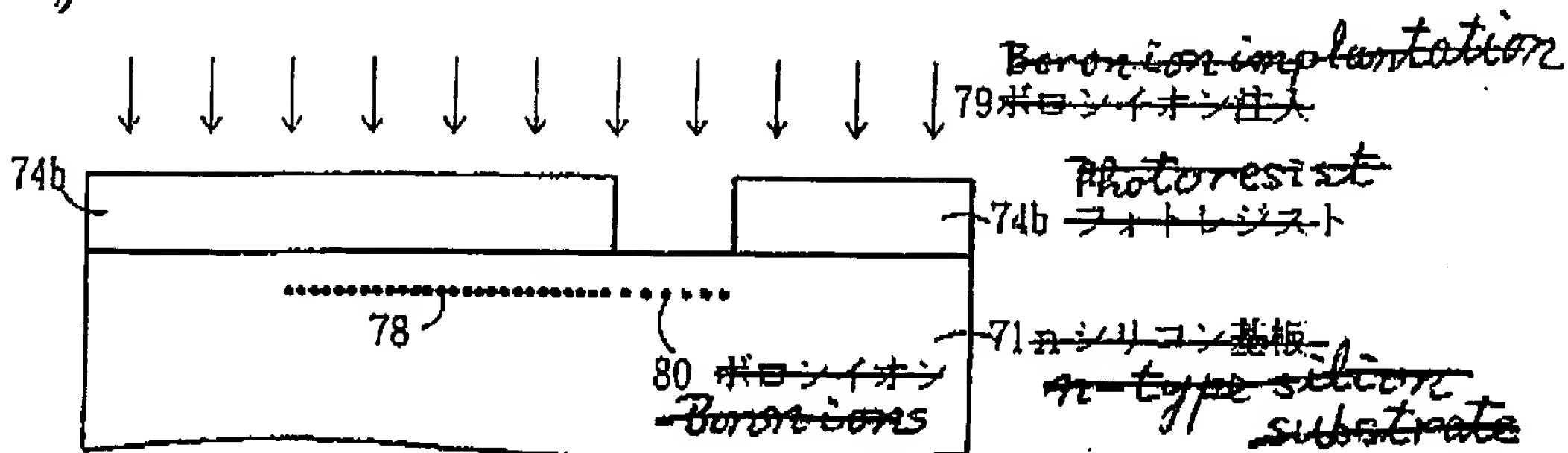


Fig. 7

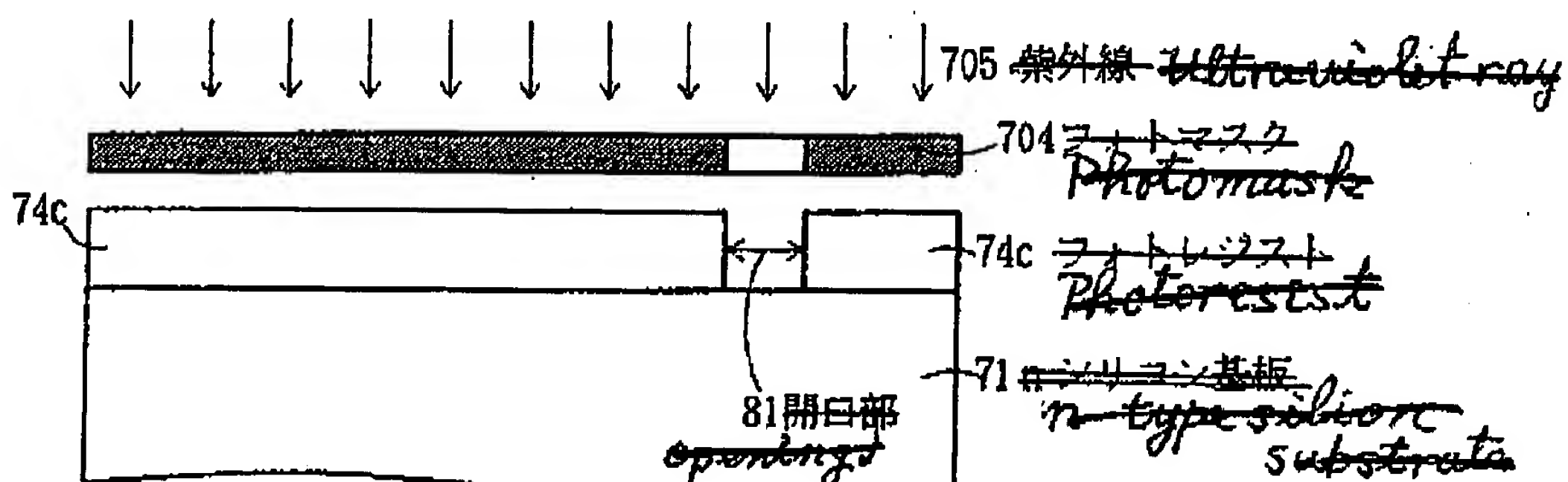


Fig. 8

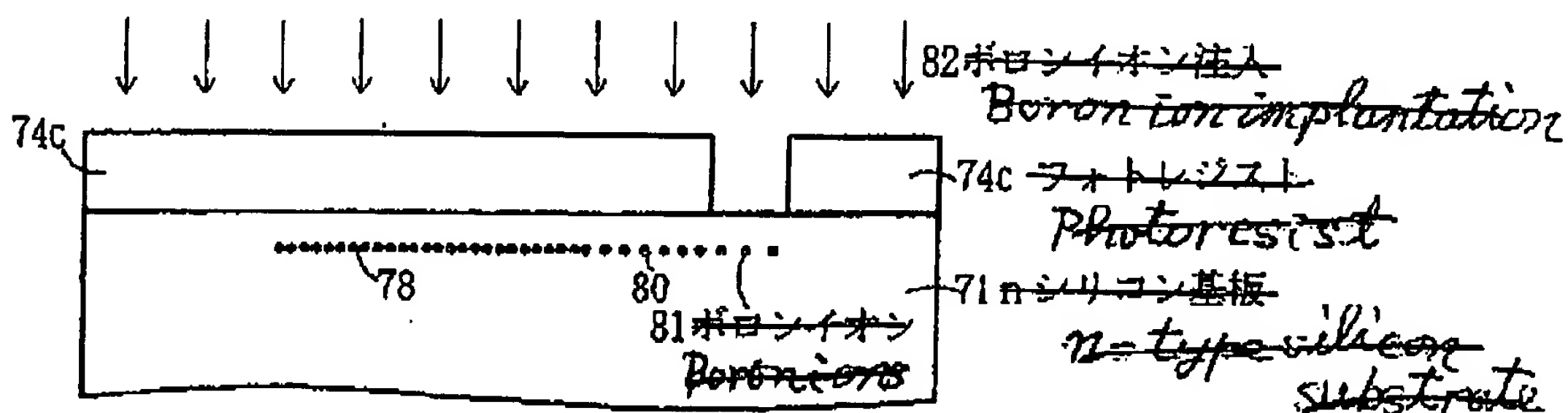


Fig. 9

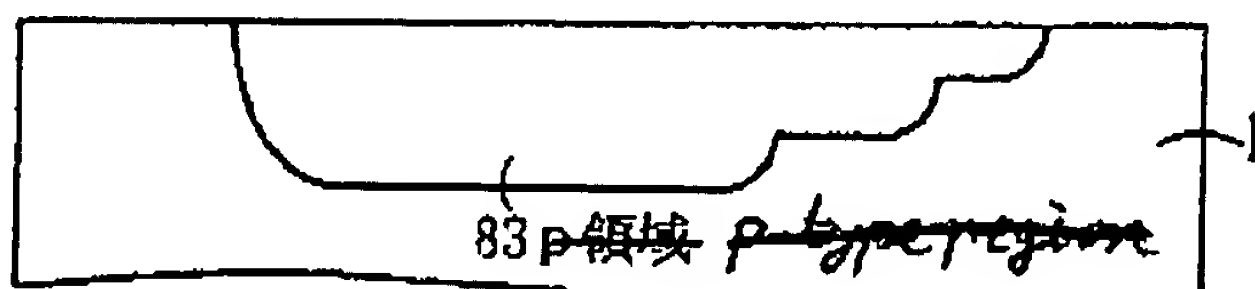


Fig. 10

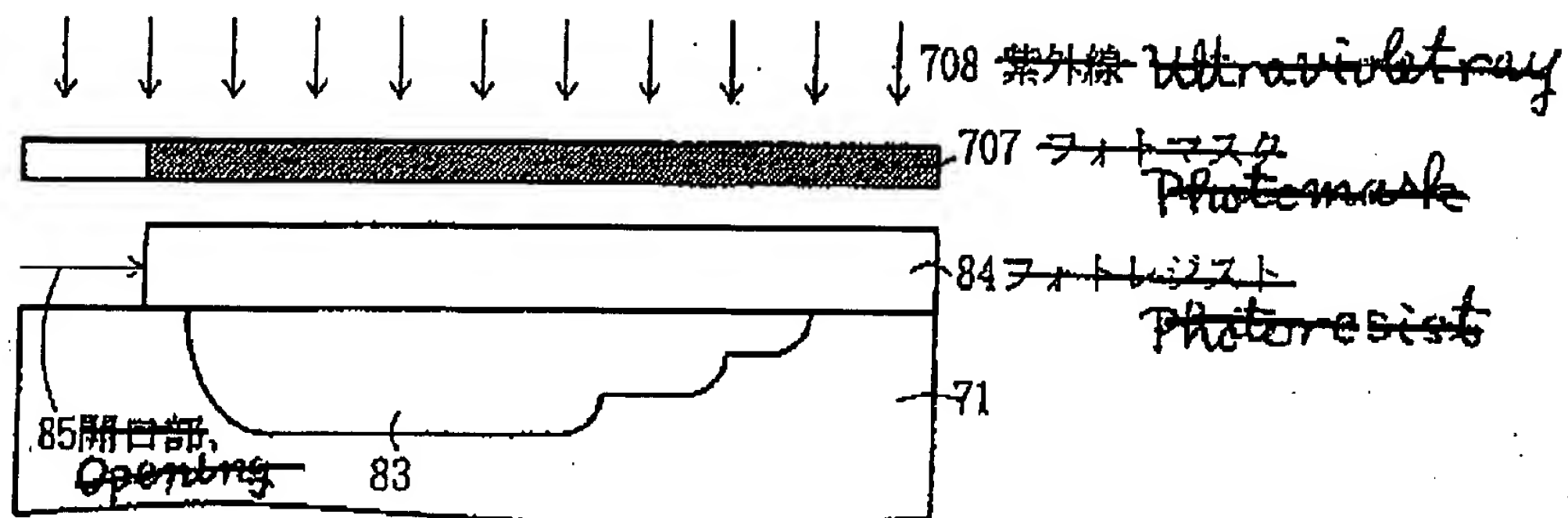


Fig. 11

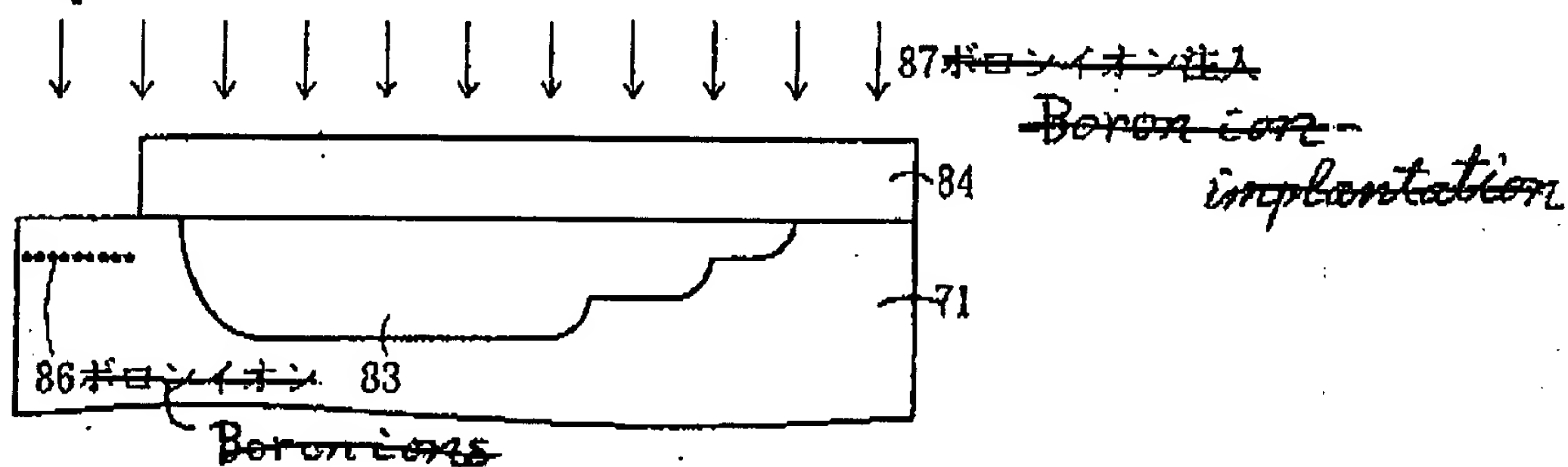
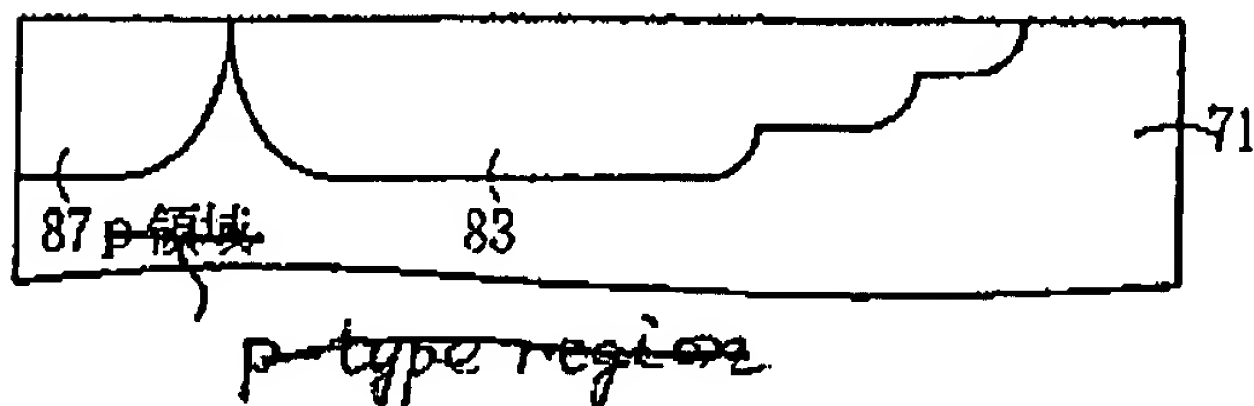
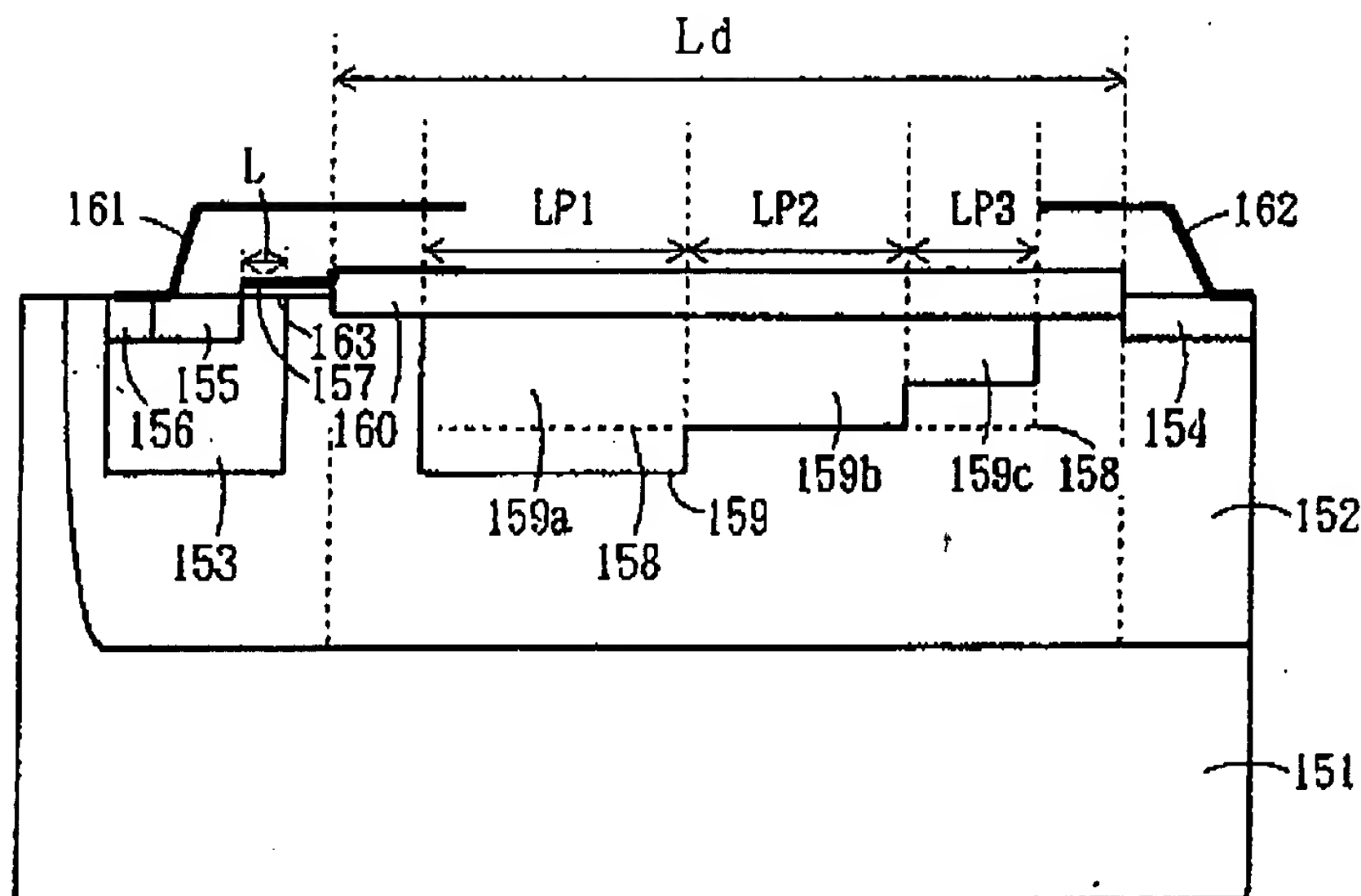


Fig. 12



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Fig. 13



- ~~151: p type substrate~~
- ~~152: n type well region~~
- ~~153: p type base region~~
- ~~154: n type drain region~~
- ~~155: n type source region~~
- ~~156: p type contact region~~
- ~~157: Gate electrode~~
- ~~158: Boron diffusion depth~~
- ~~159: p type diffusion region (p type offset region)~~
- ~~159a: First p type sub region~~
- ~~159b: Second p type sub region~~
- ~~159c: Third p type sub region~~
- ~~160: Insulation film~~
- ~~161: Source electrode~~
- ~~162: Drain electrode~~
- ~~163: Gate insulation film~~

Fig. 14

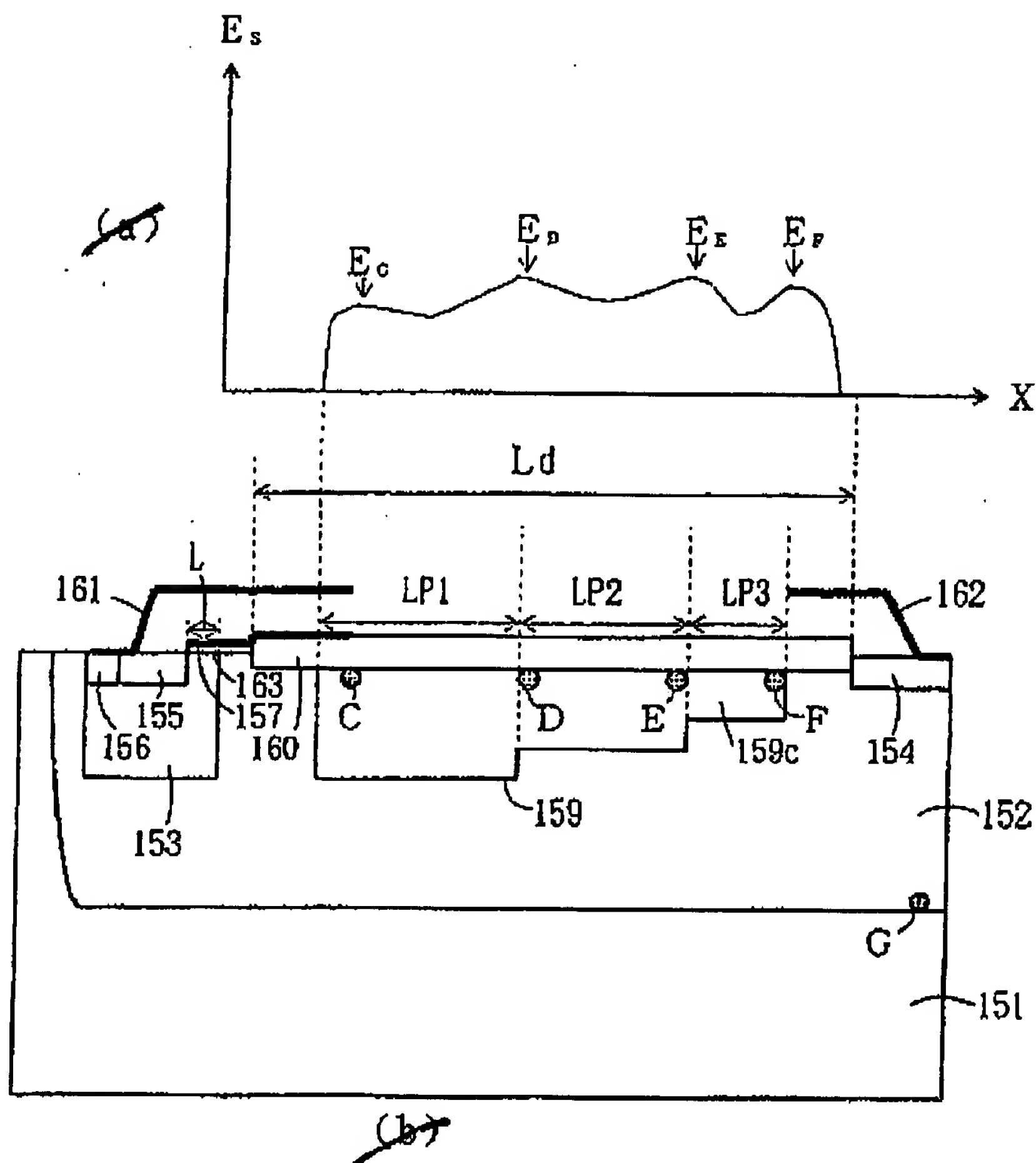
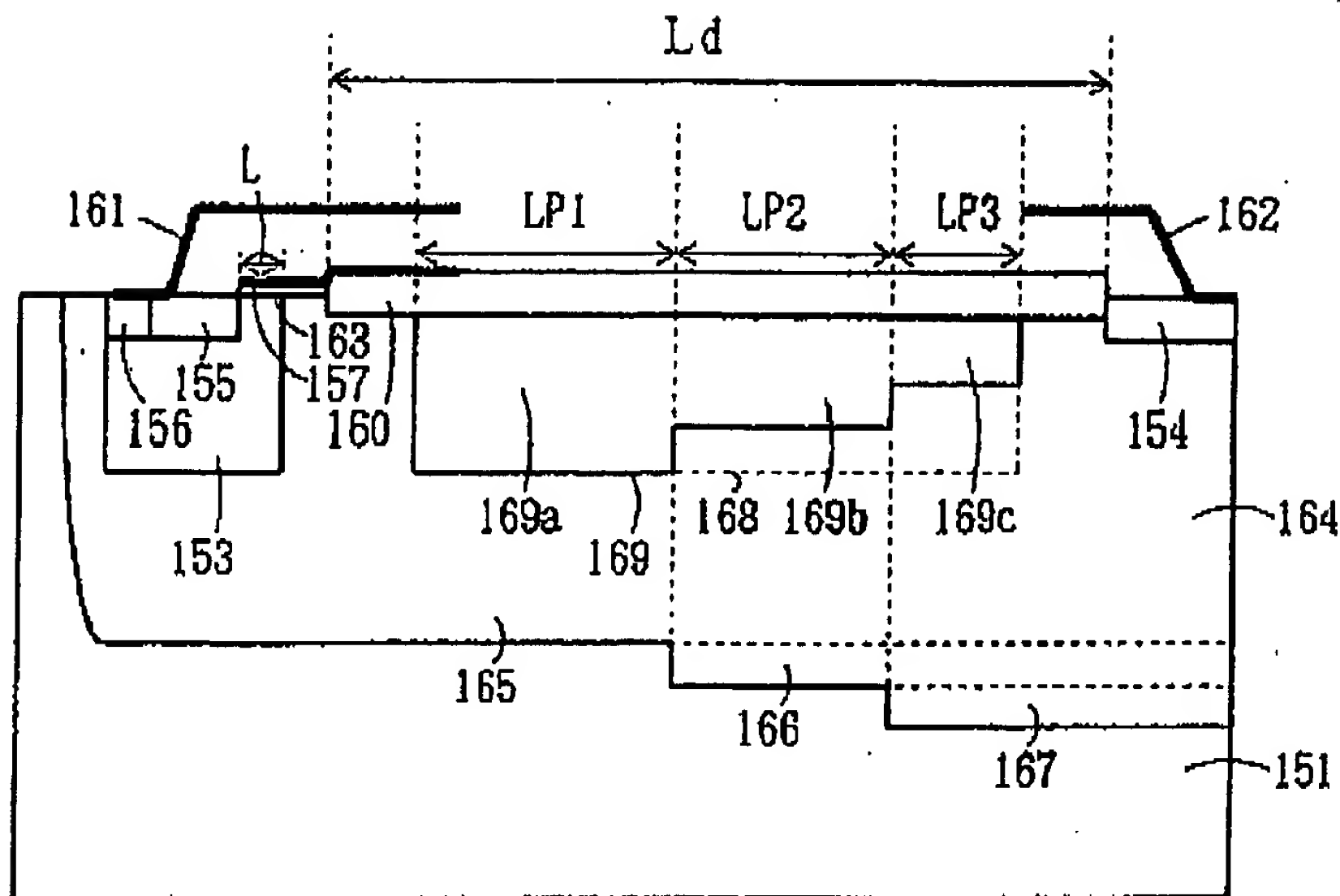


Fig. 15



- ~~164: n-type well region~~
- ~~165: First well sub-region~~
- ~~166: Second well sub-region~~
- ~~167: Third well sub-region~~
- ~~168: Boron diffusion depth~~
- ~~169: p-type diffusion region~~
- ~~169a: First p-type sub-region~~
- ~~169b: Second p-type sub-region~~
- ~~169c: Third p-type sub-region~~

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Fig. 16(a)

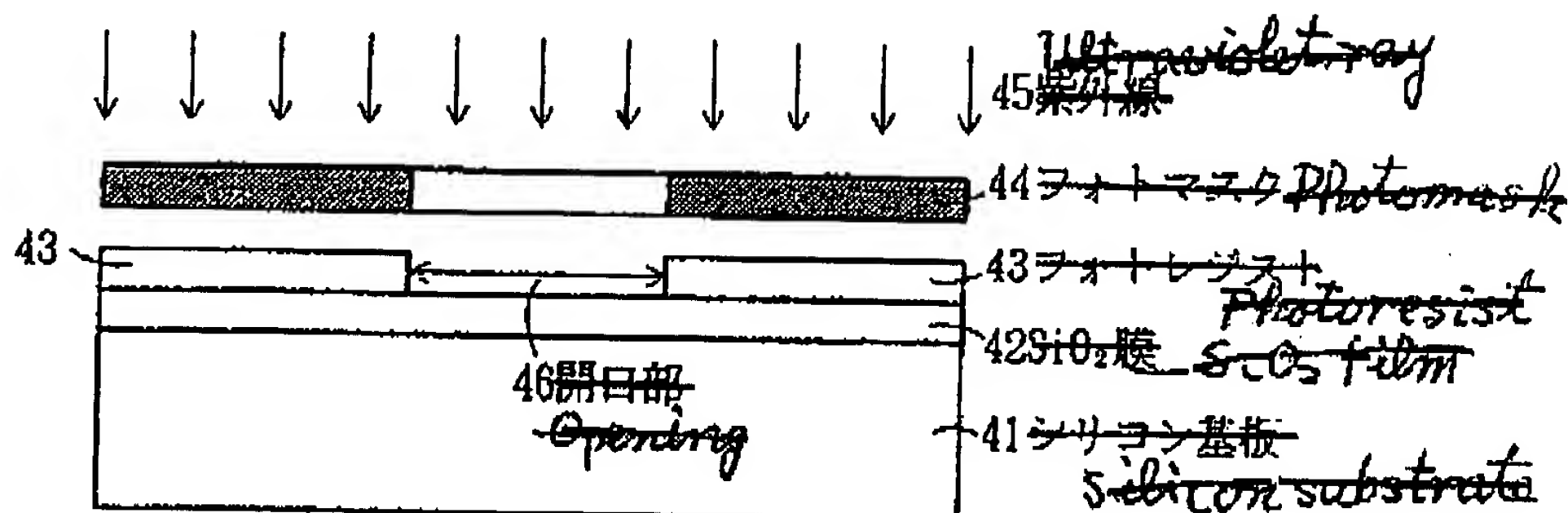


Fig. 16(b)

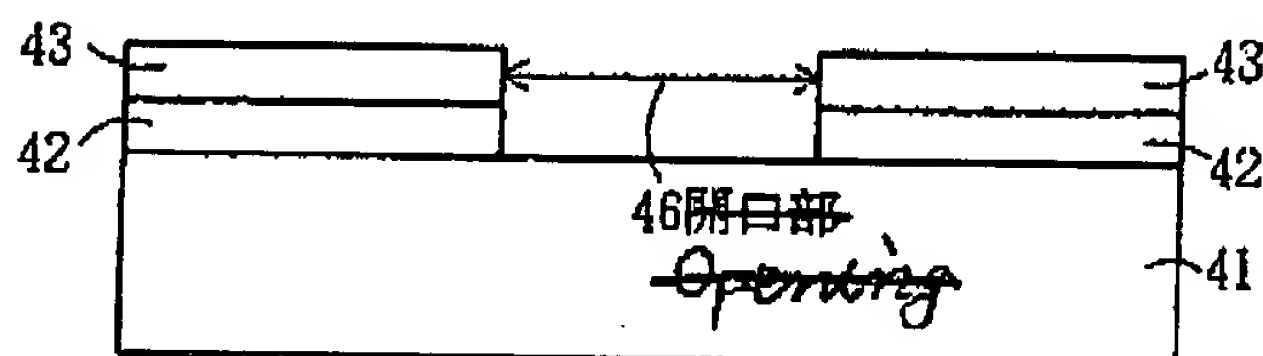


Fig. 16(c)

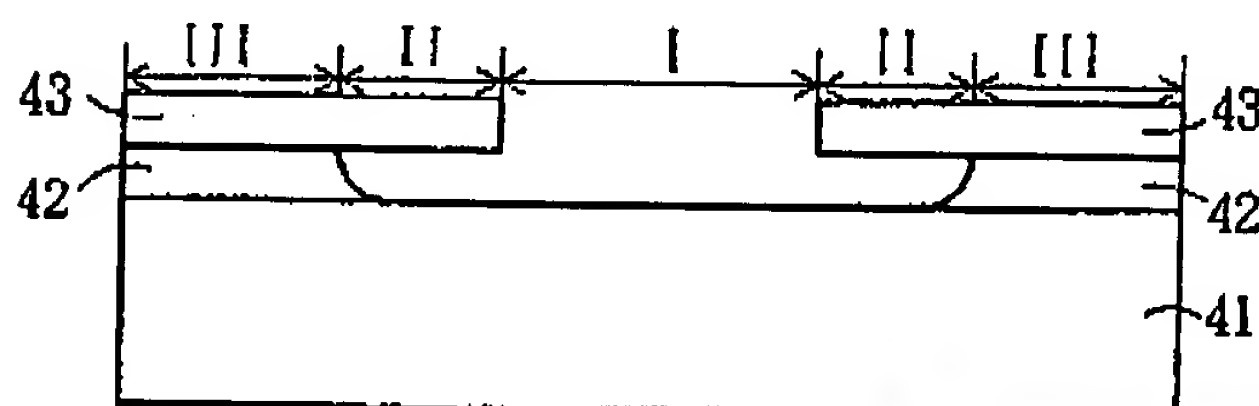


Fig. 16(d)

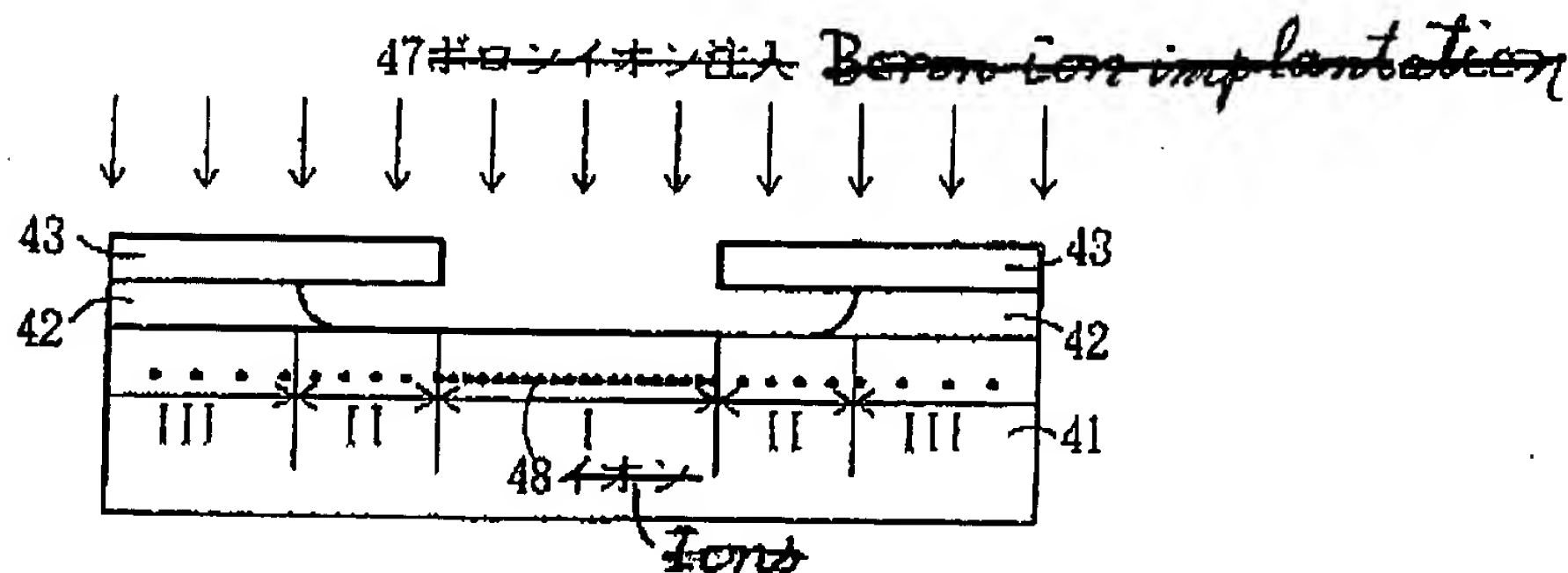
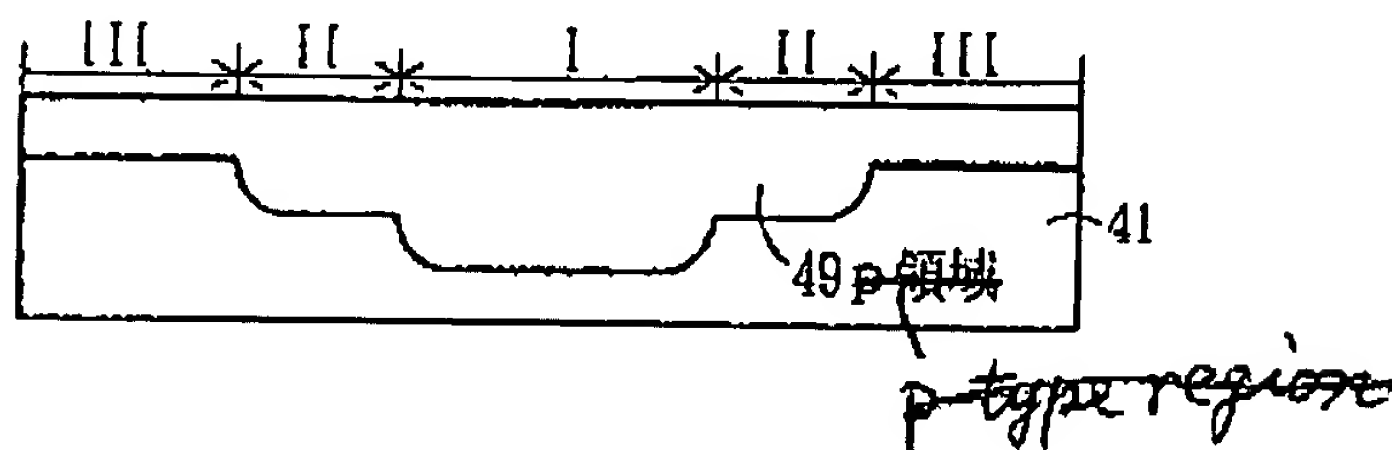
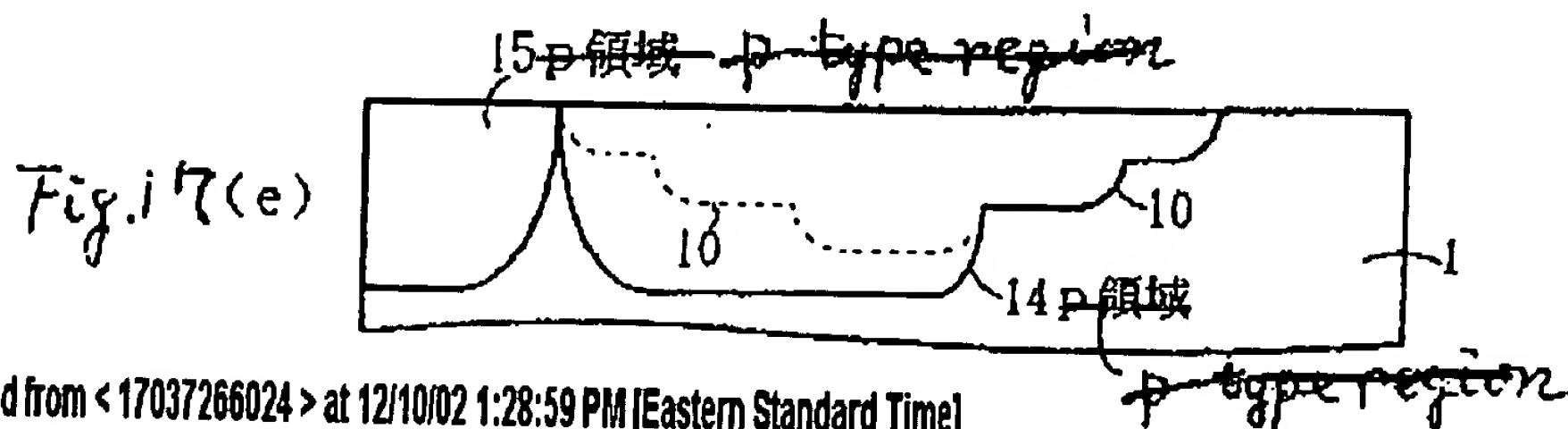
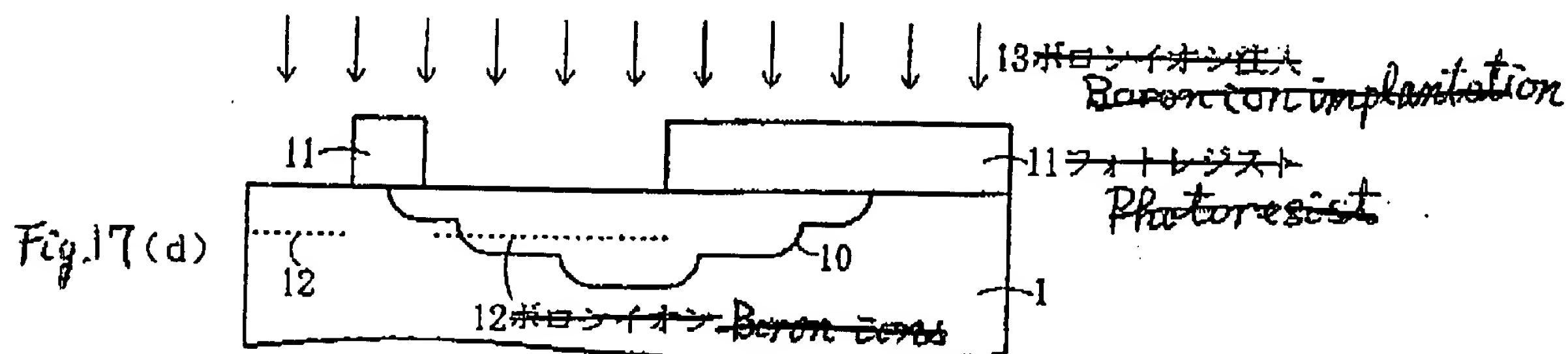
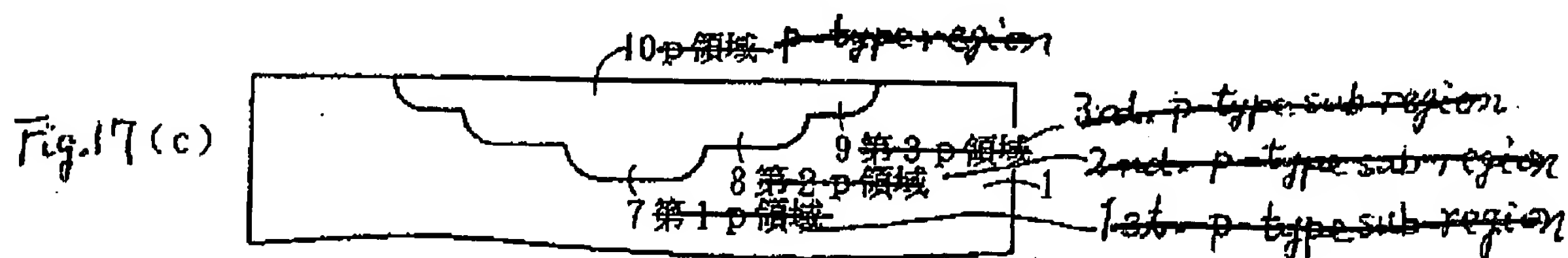
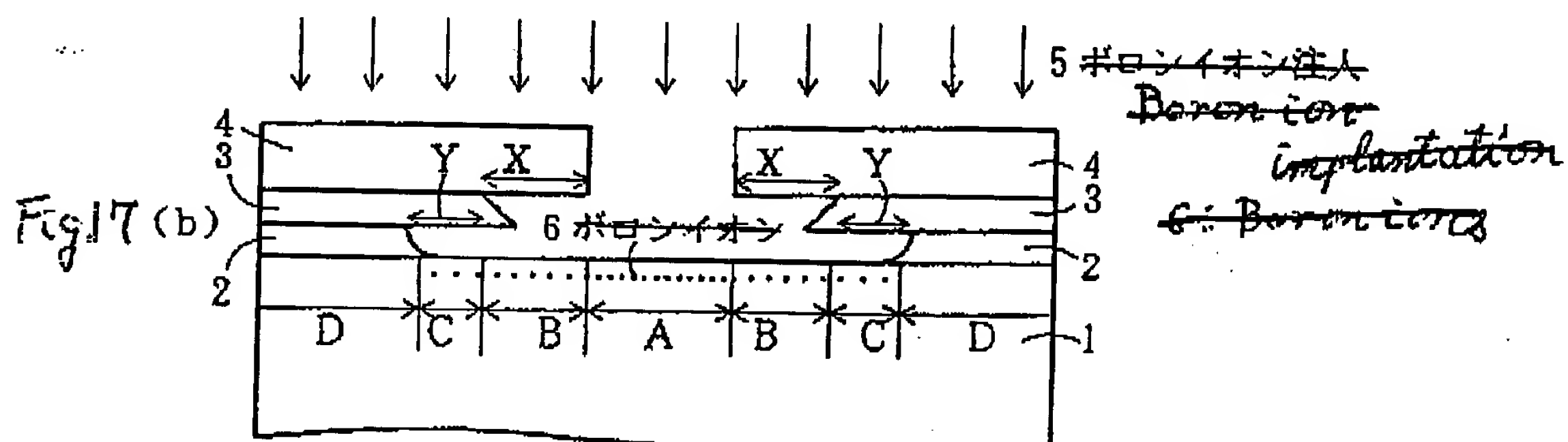
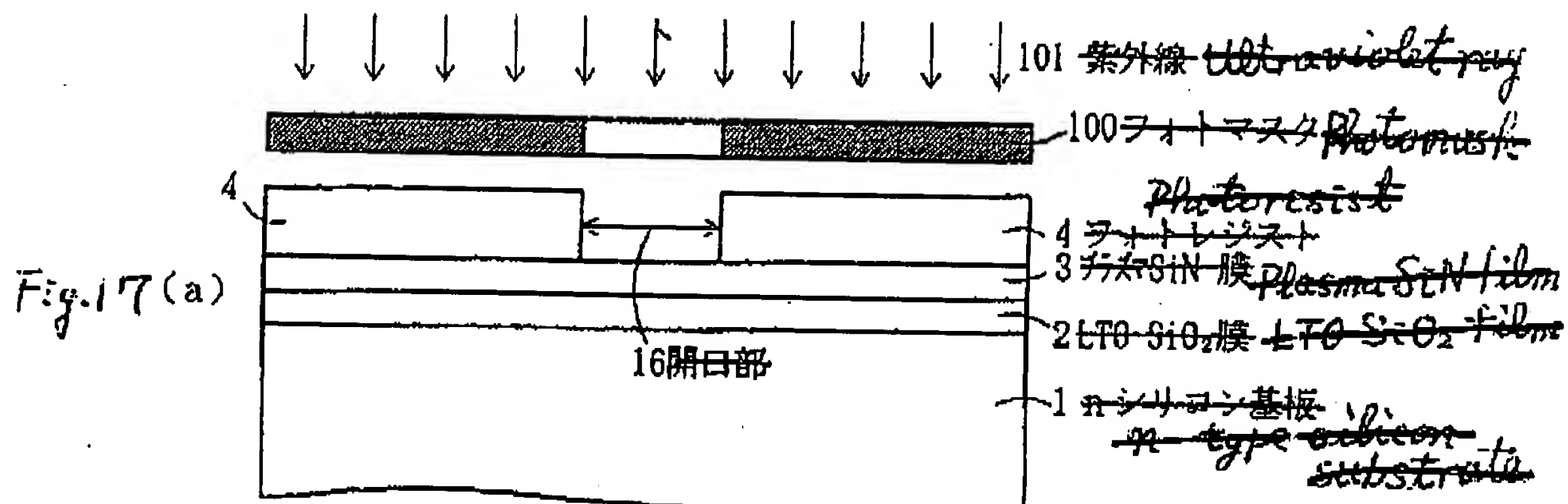


Fig. 16(e)



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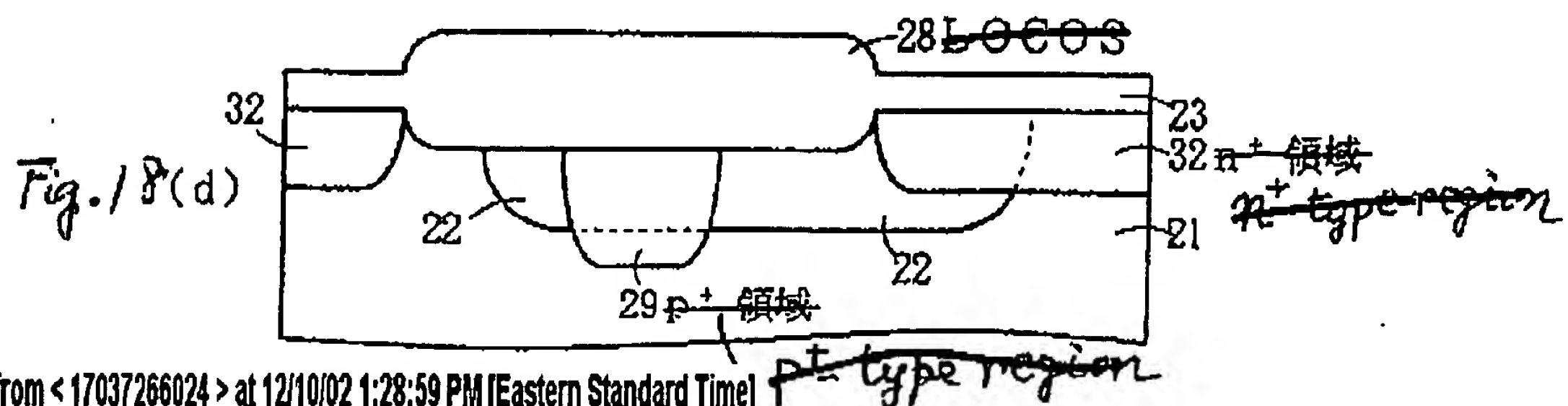
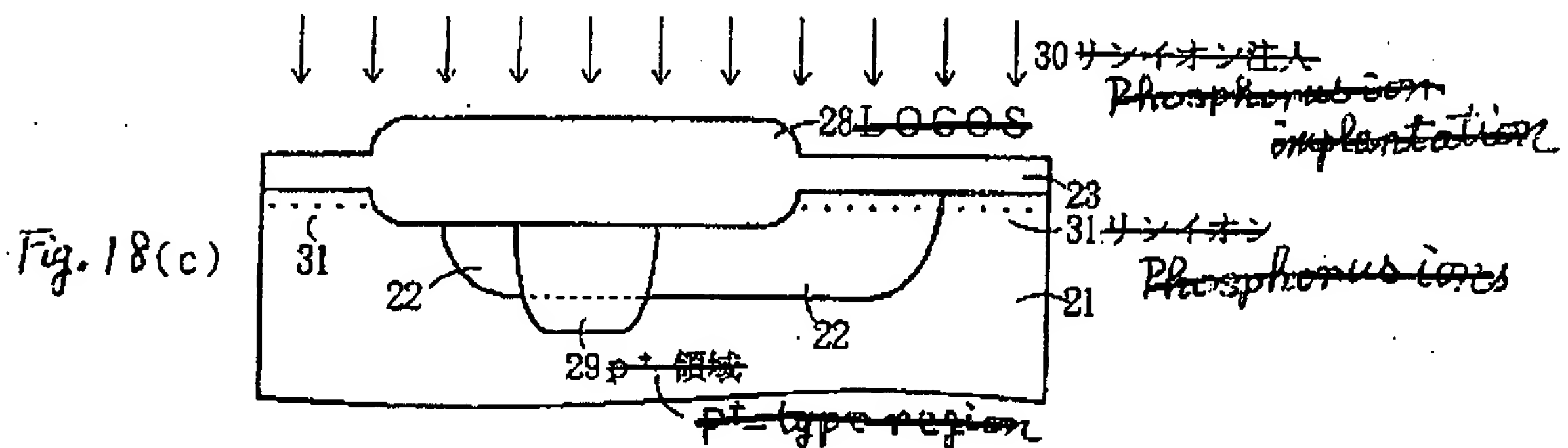
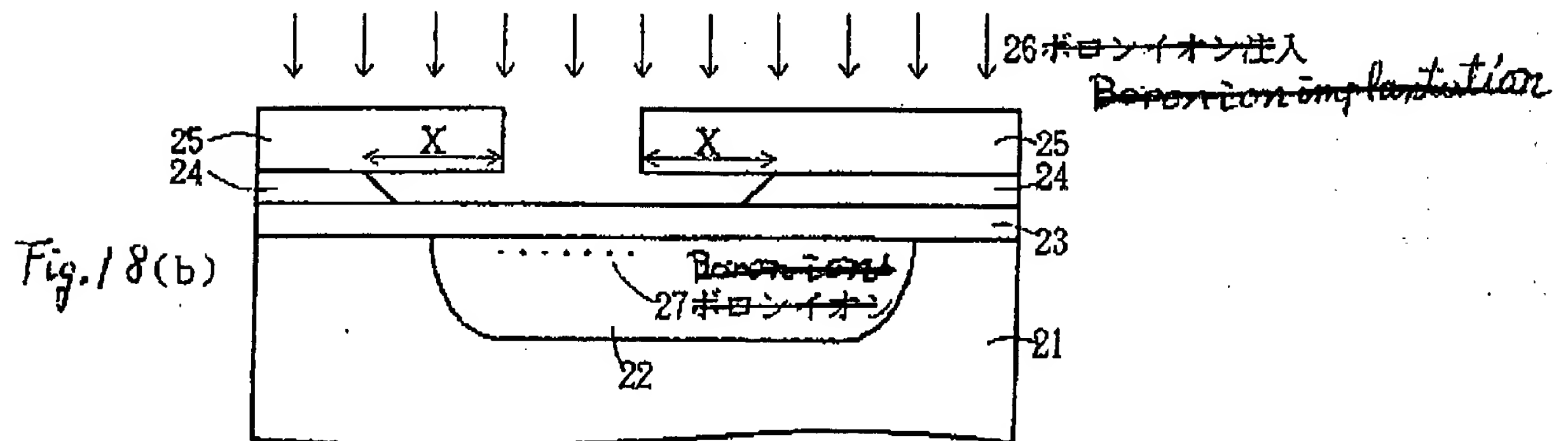
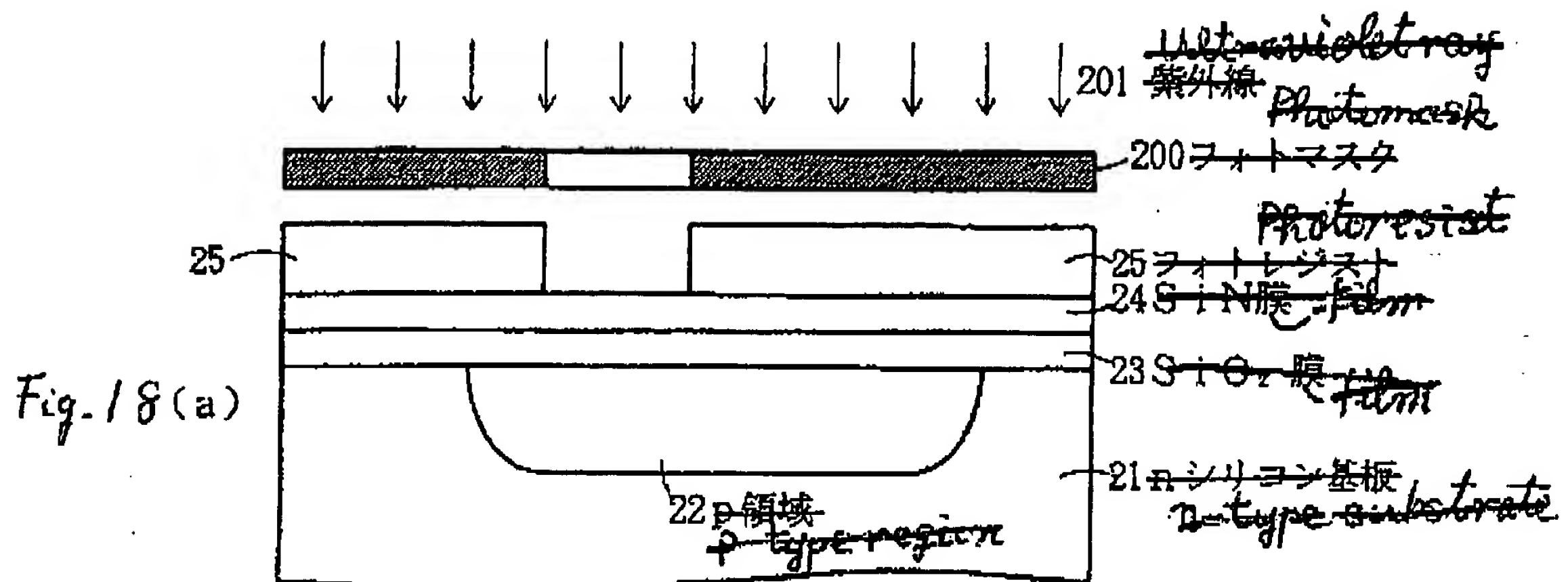
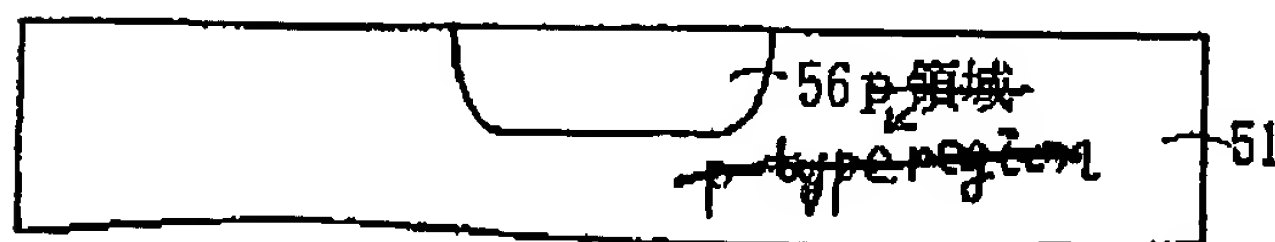
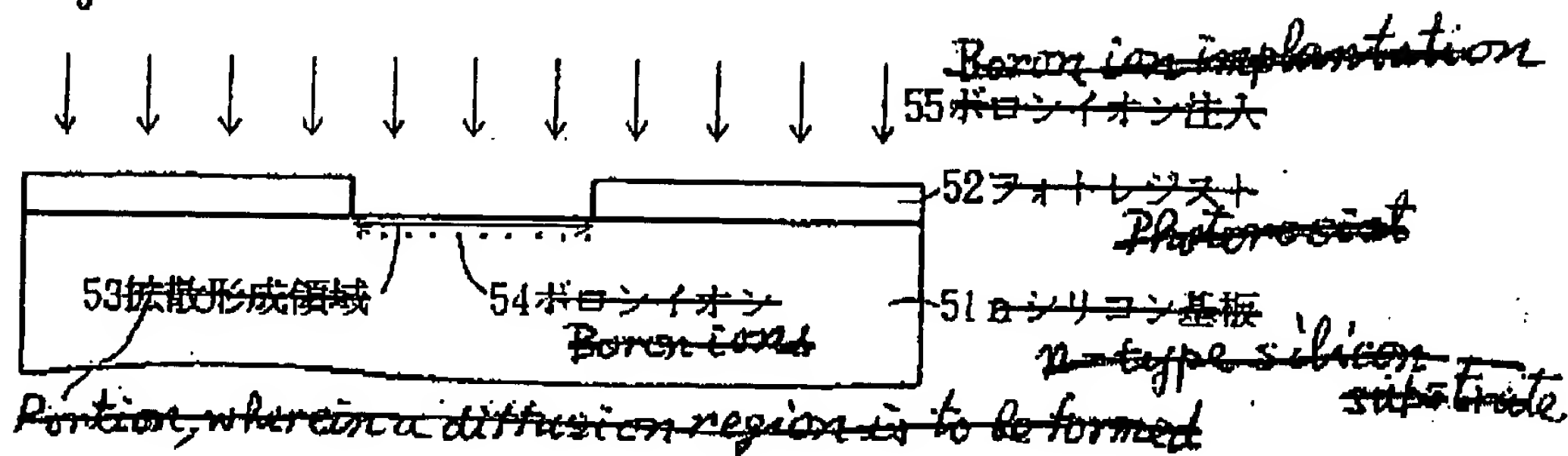
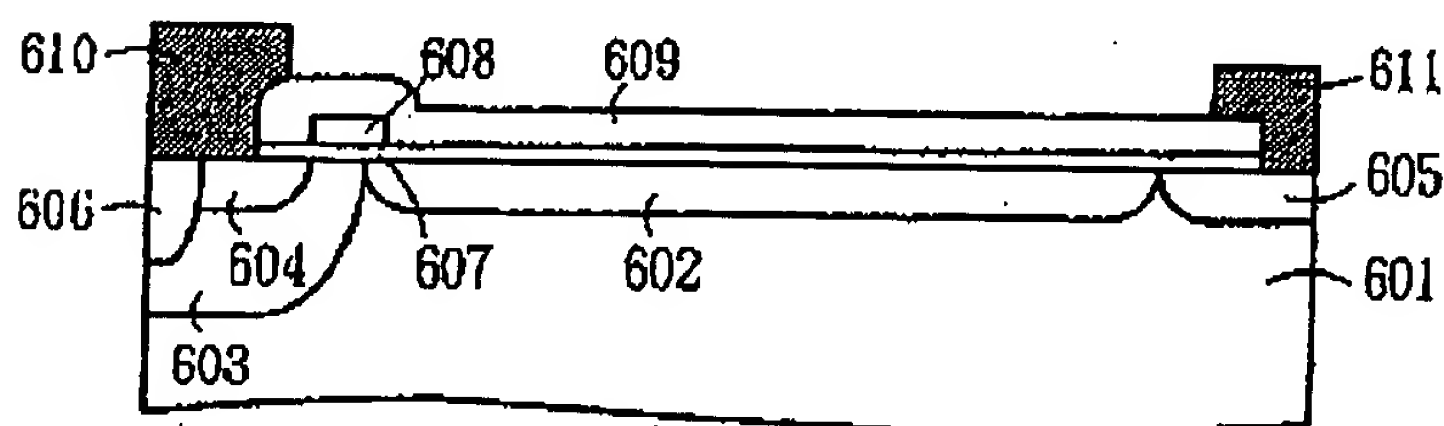


Fig. 22(a) (Prior Art)

Fig. 22(b)
(Prior Art)Fig. 23
(Prior Art)

~~601: n-type silicon substrate~~
~~602: p-type region (p-type offset region)~~
~~603: p-type region (p-type base region)~~
~~604: n-type source region~~
~~605: n-type drain region~~
~~606: p-type contact region~~

~~607: Gate oxide film~~
~~608: Gate electrode~~
~~609: Insulation film~~
~~610: Source electrode~~
~~611: Drain electrode~~

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Fig. 24
(Prior Art)

